76. The memory as claimed in claim 73, further comprising an erasing circuit to erase contents of all of said memory cells accessible by a common sector address in response to an erasing signal.

77. The memory as claimed in claim 74, wherein said first group of memory cells and said second group of memory cells are accessed by a common sector address.

78. The memory as claimed in claim 77, further comprising an erasing circuit to erase contents of all of said memory cells accessible by a common sector address in response to an erasing signal.--

REMARKS

These remarks are in response to the Office Action mailed on December 20, 1999. A Request for Declaration of Interference follows the discussions the rejection of claims 68-74. Additionally, several new claims have been added.

The Office Action rejected claims 68-74 under 35 U.S.C. 103(a) as being unpatentable over the single reference of Nakada, Japanese Patent Document No. 62-283497. It is respectfully submitted that the pending claims are not obvious over *Nakada* and that the Office Action has incorrectly identified elements and assumed structure not present. An improved translation of *Nakada* has been included: it is believed to be both more accurate and easier to read.

Claims 68,71, and 74

First, concerning claims 68, 71, and 74, these all have memory cells divided into two groups, the first group storing data and the second group storing "attribute data" of this first group, and that both of these groups are part of a specific larger structure. The figures of *Nakada* are all schematic and indicate a particular sort of file-like structure for managing the number of rewrites. Both at the time *Nakada* was written as well as at present, there are in use a number of differing techniques for storing attribute data in different ways and in different locations. The Office Action is assuming a particular structure that is neither shown nor described in *Nakada*.

Additionally, concerning claims 68 and 74, the "number of rewriting" is misidentified. In these claims, the second group of memory cells store "attribute data of said first group of memory cells", where the first group stores data. The cited quantity "write count WCNT" of *Nakada* is the number of times that the *pointer block*, not the *data*, has been rewritten. This is described, for example on page 7, lines 13-20 (of the newly sent translation) of *Nakada* :

> In the event that the write count WCNT of the pointer block 1a exceeds 10,000, data other than the write count WCNT data is transferred to the closest spare pointer block among the spare pointer blocks SPB1 through SPB50, and the write count WCNT (0000_{16}) of the new pointer block is incremented by one, to (0001_{16}). At this point the write count WCNT of the new pointer block 1a is less than 10,000. In this way, write [and] erase [operations] to the counter block 30 [sic] and the pointer block 1a are managed.

With regards to claim 71, this contains the limitation of "wherein said first group of memory cells are memory cells storing 512 bytes". It should be noted that it is the first group of memory cells, not the total plurality of memory cells, which would be the combined first and second group. Thus, the total number of the total plurality of memory cells is 512 bytes plus the number of the second group of cells with attribute information. *Nakada* instead describes an arrangement where the total number of cells is 256 bytes, with 253 being used for data. Although these numbers are taken as example in *Nakada*, this involves not just a simple numerical difference, but a conceptual difference: By taking the total number of cells to be 2^n for some n, the number of cells in the first group that is assigned for data is 2^n *minus* some number. In contrast, in claim 71 the number of *data* cells is 2^n for some n, so that the second group of cells adds to this number for a total of cells which is 2^n *plus* some number. Thus, the plurality of memory cells, composed of both the first and second groups is not the traditional 2^n for some n as in *Nakada*. In particular, *Nakada* neither describes nor suggests the use for 512 ($=2^9$) bytes for data, the significance of which is described in the present application on page 13 starting at line 7, so that the total number of memory cells is then greater than this 2^n value (cf. Figure 5).

Claims 69 and 73

Both of these claims contain the limitation "wherein said first group of memory cells and said second group of memory cells are accessed by a common sector address." Concerning this

limitation, the Office Action states: "In Fig 2, Nakada shows that his first group of memory cells and his second group of memory cells are accessed by a common sector address [i.e., they are in the same row]." Figure 2 of *Nakada* does show a block of cells as being a single row, but this is just a schematic illustration used to describe the memory management method disclosed in the document. There nothing to suggest that these cells, either just this "first group ... storing data" or the combined first and second group, are "accessible by a common sector address." *Nakada* contains no such description or suggestion of a such a sector structure, much less that the row of Figure 2 corresponds to such a sector---or even that it corresponds to a physical word or bit line. Both at the time *Nakada* was written as well as currently, there are many arrangements for where to place attribute-type information, with many schemes holding this information elsewhere than in the same sector as any related data.

Claims 70 and 72

Concerning these claims, the Office Action states: "It is conventional that a memory is provided with an erasing circuit to erase contents of all of said plurality of memory cells in response to an erasing signal." Again, *Nakada* has no discussion of an erasing circuit: In particular, it has no indication or suggestion of this particular arrangement of an erasing circuit. Given how common FLASH memory architecture has become at present, such an arrangement as given in the claims may seem conventional, but this is believed to be an application of hindsight. As with the other pending claims, these must be considered in terms of the appropriate time frame and not as seen from the present. Additionally, there exist many arrangements for placement of the attribute data, and the Office Action is assuming in its comments, as with the other claims, a particular structure.

Therefore, these rejections of claims 68-74 under 35 U.S.C. 103(a) over only *Nakada* as a single reference are respectfully traversed. It is admitted in the Office Action that these claims recite some feature which *Nakada* "does not teach" or, although absent, is assumed to be inherent or "conventional". Yet there is no further reference or other evidence of prior art presented to demonstrate that the overall claimed combinations including the elements missing from *Nakada* would have been obvious. The Office Action either summarily states that "it would have been obvious" to

add the missing element to *Nakada* in order to meet the terms of the claims, or that the elements missing from *Nakada* are inherent in *Nakada* and would have been obvious to include in the claimed combinations. In either case, assumptions have improperly been made by the Examiner as to what one ordinarily skilled in the art would have found obvious to do since there is no supporting evidence provided in the Office Action. It is respectfully submitted that these rejections do not make the necessary *prima facie* case of obviousness, and that, on that basis, the rejection of claims 68-74 must be withdrawn.

New Claims

Several new claims have been added to highlight features application which are absent from *Nakada* and the other prior art. Claims 75 and 76 depend respectively upon claims 69 and 73 and add "an erasing circuit to erase contents of all of said memory cells accessible by a common sector address in response to an erasing signal." As noted above, such a structure is neither taught nor suggested by *Nakada*. New claims 77 and 78 are the same as the pair 69 and 75 or the pair 73 and 76, but depend upon claim 74 as their base claim.

Consideration of these new claims, as well as reconsideration of the Office Action's rejection of claims 68-74, is therefore respectfully requested, and an early indication of their allowability is earnestly solicited.

REQUEST FOR DECLARATION OF INTERFERENCE

It is respectfully requested that an interference be declared between the present application and U.S. patent no. 5,818,754 of Ogura, referred to below as the "'754 patent". Independent claims 68 and 74 are exact copies of claims 7 and 18, respectively, of the '754. Independent claim 71 is an exact copy of claim 12 of the Ogura patent, except that the last word "bits" of the patent claims has been changed to "bytes." This change makes claim 12 consistent with the disclosure the present application. The Ogura patent describes sectors having a data capacity of either 512 bits or 512 bytes. The new dependent claims being added by this Amendment are patterned after some of the dependent claims of the Ogura patent but are not exactly the same. Claim

68 of the present application, which is an exact copy of claim 7 of the `754 patent, is suggested as the count for the interference, as follows:

Count 1

A memory comprising:

a plurality of word lines;

a plurality of bit lines; and

a plurality of memory cells, wherein each of said memory cells corresponds to a selected one of said plurality of word lines and a selected one of said plurality of bit lines;

wherein said plurality of memory cells are divided into a first group of memory cells and a second group of memory cells, said first group of memory cells being provided for storing data and said second group of memory cells being provided for storing attribute data of said first group of memory cells, wherein said attribute data includes a number of rewriting of said first group of memory cells.

35 U.S.C. 135(b)

Claim 68 of the present application was added by Preliminary Amendment, simultaneously with the filing of the present continued prosecution application on September 30, 1999. This is less than one year after the `754 patent was granted on October 6, 1998.

Effective Filing Date

As specified in the "Cross-Reference to Related Application" section added by the Preliminary Amendment filed on August 28, 1998, to the beginning of the application of which the present application is a continued prosecution application, the present application is entitled to an effective filing date of April 13, 1989 due to the benefit of:

U.S. Ser. No. 08/771,708, filed December 20, 1996,

U.S. Ser. No. 08/174,768, filed December 29, 1993, now patent no. 5,602,987,

U.S. Ser. No. 07/963,838, filed October 20, 1992, now patent no. 5,297,148,

U.S. Ser. No. 07/337,566, filed April 13, 1989.

The `754 patent is shown to have a United States filing date of December 27,1996, claiming priority from a Japanese patent applications with a date of December 27,1995. This over six years later than the April 13, 1989 effective filing date of the present application.

Therefore, it is requested that the interference be declared with the Applicants of the present application designated the senior party.

Claims Corresponding to the Proposed Count 1

The proposed count 1 is an exact copy of claim 7 of the `754 patent. Claims 8 and 11 respectively add addressing and erasing details. Independent claim 18 corresponds to claim 7, differing only slightly in its limitations

Support for the Proposed Count 1 in the Present Application

The present application incorporates U.S. patent no. 5,095,344 ('344 patent) of Dr. Harari by reference on page 11, line 26, and page 22, line 14, and mentions it again on page 26. It is the combination of the present application specification and the incorporated '344 patent which provides support for claim 68 as well as claims 69-74.

Count 1	Present Application
A memory comprising: a plurality of word lines; a plurality of bit lines; and a plurality of memory cells, wherein each of said memory cells corresponds to a selected one of said plurality of word lines and a selected one of said plurality of bit lines;	Figures 15a and 15b of `344 show such a memory, with each cell corresponding to a selected one of the rows (word lines) and a selected one of the columns (bit lines). The structure is discussed in section VIII of the `344 patent beginning at column 32, line 57.

wherein said plurality of memory cells are divided into a first group of memory cells and a second group of memory cells, said first group of memory cells being provided for storing data and said second group of memory cells being provided for storing attribute data of said first group of memory cells, wherein said attribute data includes a number of rewriting of said first group of memory cells.

Figure 5 of the present application, described beginning at page 16, line 23, describes such a division into portions 403 and 405. Figure 12 of `344 and its description beginning at col. 28, lns. 36 describe storing in an individual sector the number S of program/erase cycles: "The value of S at any one time can be stored ... in each block. That way each block carries its own endurance history."(`344, col. 29, lns. 3-7)

Examples of the attribute data are given in the present application with respect to the Figure 5 sector partition diagram. In addition to user data, which is described to be 512 bytes of data as a specific example, an individual sector may contain data of defects of the sector. The incorporated '344 patent additionally describes storing in an individual sector the number S of program/erase cycles which has been experienced by that sector. (see Fig. 12 and the description beginning at col. 28, lns. 36, for example.)

For these reasons, it is submitted to be clear that claim 7 of the `754 patent is supported by the present application disclosure, first filed on April 13, 1989.

`754 Patent Prosecution File History

A review of the file history of the `754 patent reveals that the material in the neither the present application nor any of its descendants was cited during the `476 patent application process. However, U.S. patent number 5,268,870, which is a division of U.S. patent number 5,095,344 of Harari that is included by reference in the present application, was cited during the `754 patent application process. This patent was cited but not relied upon in the first Office Action mailed on May 15, 1997, being briefly noted in the Conclusion as follows: "Harari (5,268,870) discloses a flash EEPROM system and intelligent programming and eraing [sic.] methods therefor [sic.]." Beyond this, it is not discussed in any of the Office Actions or Amendments.

Conclusion

A prompt declaration of the requested interference is respectfully requested. In the meantime, however, if the Examiner has any questions about this request, application or disclosure statements, a telephone call to the undersigned is invited.

Dated: March 17, 2000.

Respectfully submitted,

By: _____

Michael G. Cleveland, Reg. No. P46,030
MAJESTIC, PARSONS, SIEBERT & HSUE P.C.
Four Embarcadero Center, Suite 1100
San Francisco, California 94111-4106
Telephone: (415) 248-5500
Facsimile: (415) 362-5418

Atty. Docket: HARI.006UST